

Notice of References Cited	Application/Control No. 09/840,500	Applicant(s)/Patent Under Reexamination TSAI, ROGER S.	
	Examiner Thomas H. Stevens	Art Unit 2123	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
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	B	US-5,966,520	10-1999	Buer et al.	716/6
	C	US-6,133,132	10-2000	Toprac et al.	438/595
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	L	US-			
	M	US-			

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NON-PATENT DOCUMENTS

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	U	Muller et al., Device Electronics For Integrated Circuits 2 nd Edition 1986. pg. 475-516.
	V	Biswas-B ., "Modeling and Simuation of High Speed Interconnects" Dissertation-- University of North Carolina State. 1998. pg. 1-67.
	W	VTT Electronics. "Research Activities in Mircoelectronics 2000" 2000. pg. 1-71.
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.